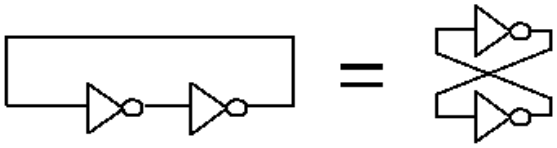
The Flipflops

The Basic Memory Cell: Latches

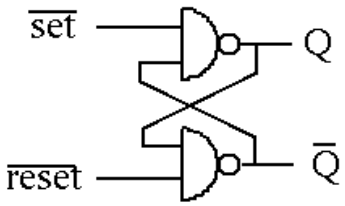
Feedback is the key to having memory capability. Here is the simplest circuit that can remember one bit of information:



Two types of latches can be built by using either NAND or NOR gates. First recall the basic logic of these gates:

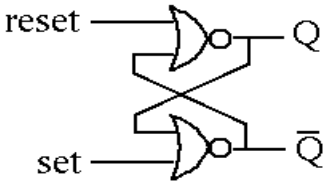
A	B	$(AB)'$	$(A+B)'$
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	0

NAND latch



$\overline{set}$	$\overline{reset}$	Q_{t+1}	$\overline{Q}_{t+1}$	
0	0	1	1	
0	1	1	0	(set or preset)
1	0	0	1	(clear or reset)
1	1	Q_t	$\overline{Q}_t$	(no change: $Q_t = Q_{t+1}$)

NOR latch

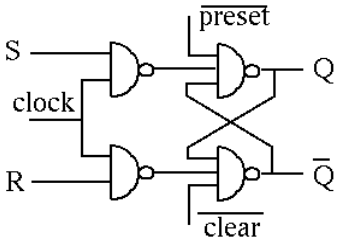


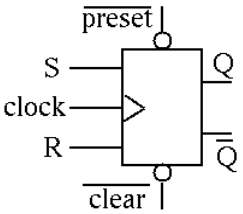
set	reset	Q_{t+1}	$\overline{Q}_{t+1}$	
0	0	Q_t	$\overline{Q}_t$	(no change: $Q_t = Q_{t+1}$)
0	1	0	1	(reset)
1	0	1	0	(set)
1	1	0	0	

Clocked Latches: Flipflops

RS-Flipflop (Set-Reset):

Clock	S	R	$\overline{set}$	$\overline{reset}$	Q_{t+1}	$\overline{Q}_{t+1}$	
0	x	x	1	1	Q_t	$\overline{Q}_t$	(no change)
1	0	0	1	1	Q_t	$\overline{Q}_t$	(no change)
1	0	1	1	0	0	1	(reset)
1	1	0	0	1	1	0	(set)
1	1	1	0	0	1	1	(not allowed *)





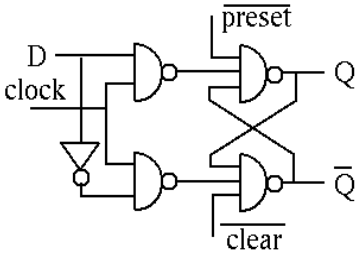
S R	Q_{t+1}
0 0	Q_t
0 1	0
1 0	1
1 1	not allowed

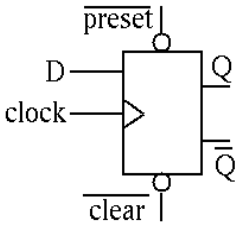
S and *R* are not allowed to be 1 at the same time, as the states of Q and $\overline{Q}$ are unpredictable when the clock becomes 0.

D-Flipflop (Delay)

To avoid the undesirable state S = R = 1 in an RS-FF, we let R = S' and rename S as D. Now only the middle two states in the above RS-FF remain, and the resulting circuit is a D-flipflop:

Clock	D	$\overline{set}$	$\overline{reset}$	Q_{t+1}	$\overline{Q}_{t+1}$	
0	x	1	1	Q_t	$\overline{Q}_t$	(no change)
1	0	0	1	0	1	(reset)
1	1	1	0	1	0	(set)



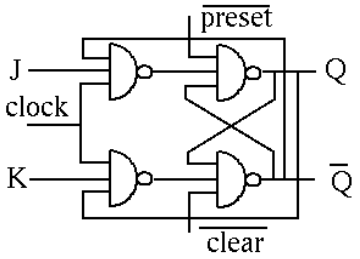


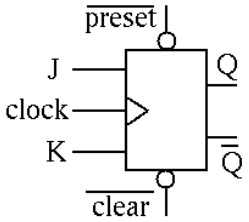
D	Q_{t+1}
0	0
1	1

JK-Flipflop

Feedback can be used as another way to avoid the unpredictable state in an RS-FF. The output Q and $\overline{Q}$ are sent back to the set and reset side, respectively, and the S and R inputs are renamed as J and K. Now Q and $\overline{Q}$ are guaranteed to be always opposite to each other.

Clock	J	K	Q_t	$\overline{Q}_t$	$\overline{set}$	$\overline{reset}$	Q_{t+1}	$\overline{Q}_{t+1}$	
0	x	x	x	x	1	1	Q	$\overline{Q}$	(no change)
1	0	0	x	x	1	1	Q	$\overline{Q}$	(no change)
1	0	1	0	1	1	1	0	1	(no change)
1	0	1	1	0	1	0	0	1	(reset)
1	1	0	0	1	0	1	1	0	(set)
1	1	0	1	0	1	1	1	0	(no change)
1	1	1	0	1	0	1	1	0	(set)
1	1	1	1	0	1	0	0	1	(reset)

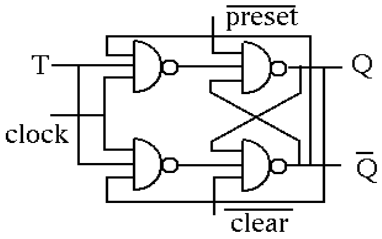


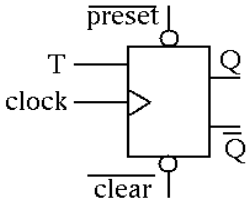


J	K	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	$\overline{Q}_t$

T-Flipflop (Toggle)

If the J and K inputs are tied together and renamed as T (for toggle), only the first and last states of JK-FF remain, and the FF becomes a toggle FF:





T	Q_{t+1}
0	Q_t
1	$\overline{Q}_t$

Summary

The different types of Flipflops (RS, JK, D and T) can also be described by their excitation table, as shown below. The left side shows the desired transition from Q(*t*) to Q(*t* + 1), and the right side gives the triggering signals needed for the transitions in various types of FFs.

Desired transition		Triggering signal needed					
Q(t)	Q(t+1)	S	R	J	K	D	T
0	0	0	x	0	x	0	0
0	1	1	0	1	x	1	1
1	0	0	1	x	1	0	1
1	1	x	0	x	0	1	0