CS1800 Discrete Structures *Out: September 12, 2026*

Problem Set 1

Strange & Varma *Due: September 18, 2026*

- This assignment is **due on September 18, 2026 at 11:59 PM** via Gradescope. You may submit up to 48 hours late with no penalty.
- Your solutions must be handwritten, with your name on the first page. All your work must be shown even if the problem doesn't specifically ask for it.
- Discussing problems with classmates is allowed but all solutions must be written by yourself, in your own words.
- Copying solutions from a classmate, an online source, or AI tools, is a violation of our academic integrity policy. Do *not* submit anything you cannot explain. Please list all your collaborators and online reference sources in your solution for each problem.
- If you get stuck on a homework problem, come by office hours or post on Campuswire! We recommend you spend about 30 minutes trying to figure out a problem, and then ask for help. We'll be happy to clarify material from class and algorithm concepts, but we will not give out solutions or confirm your answers are correct.

Problem 1 (Towards Truth) **12**

Given the logic circuit with inputs A, B, and C, make the truth table for the resulting output Y. Make sure to include a column in the truth table for all intermediate results, that is, the outputs from each gate before reaching the final output Y.

Thus, the columns in your truth table should be: A, B, C, GA1, GA2, GA3, GN1, GN2, GO1, GO2 which is the same as Y.

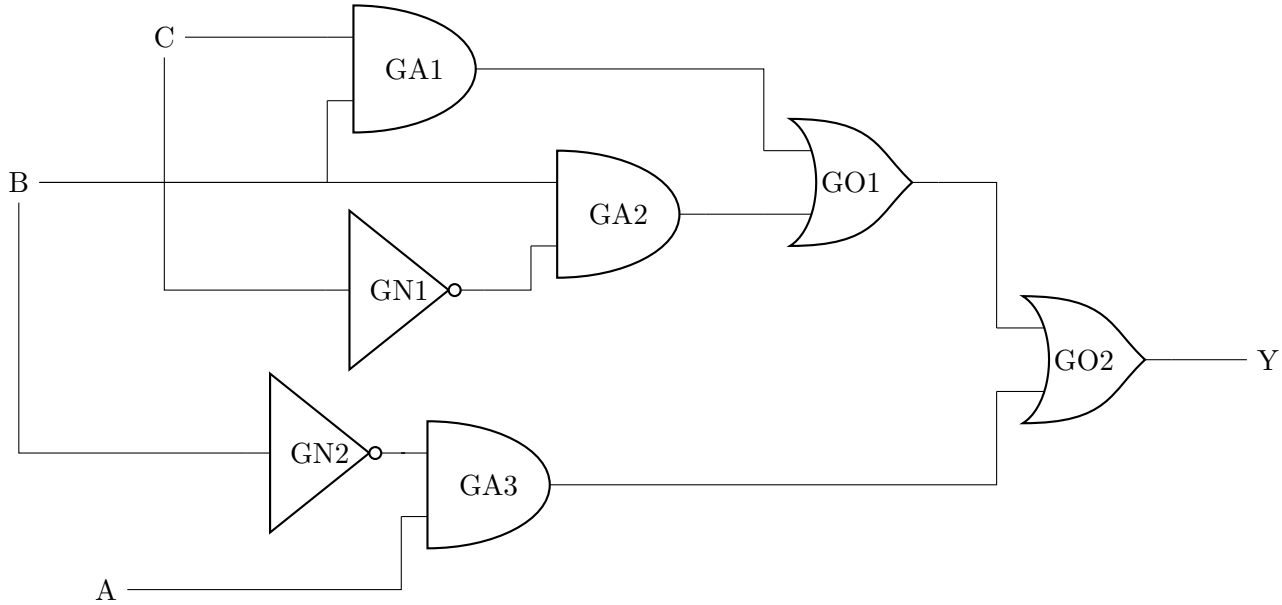


Figure 1: Given logic circuit with inputs A, B, C and final resulting output Y. The goal is to make the truth table representing this circuit.

Problem 2 (From Truth) 12

Given the truth table below, draw the logic circuit representing this. Although the truth table seems to use 4 gates (G1, G2, G3, and one before the final output), there could be "smaller" circuits if gates other than AND, OR, and NOT are used. Any valid circuit which represents this truth table is an acceptable solution.

A	B	C	G1	G2	G3	Final Output
0	0	0	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	1	0
0	1	1	1	1	0	0
1	0	0	1	0	1	1
1	0	1	1	0	1	1
1	1	0	1	0	1	1
1	1	1	1	1	0	0

Table 1: Truth table to be converted to a logical circuit.

[***Hint**: A and C depends on G1; B and C on G2; G2 on G3; the final output G1 and G3*]

Problem 3 (Making a table) 6+6

The output is 1 in either of the following two situations: (i) if C is 1. (ii) if exactly one out of A and B is 1.

For this problem, you need to do the following:

a Make a truth table for the above description, including any intermediate columns you think are necessary.

b Make the corresponding logic circuit from the truth table. You can utilize whichever gates you think are necessary.

Problem 4 (Finding the Truth) 6+6+2

An old tablet has been found in a temple of the Roman goddess Veritas, describing a partially worn out logic circuit (see Figure 2) and a partially scratched up truth table (see Table 2). The only text that can be read on the tablet mentions that the logic circuit and the truth table are equivalent. There's only one other clue: the tablet is titled "The □□□□□ gate using AND, OR, and NOT gates". Of course, the name of the gate this circuit represents has also been scratched off.[1]

Your goal is to figure out this 3-part mystery (that you might want to attempt simultaneously):

a Find out what were the unknown gates (which we have labelled U1 and U2) before they were worn out. So draw a new circuit with all gates correct, without any "unknown" gates.

b Fill out the entries marked with '?' in the partial truth table. So write out a fully filled out truth table.

c Figure out which gate is represented by this circuit. That is, what gate can directly produce the output from GO1 (last column of the truth table) given A and B as input.

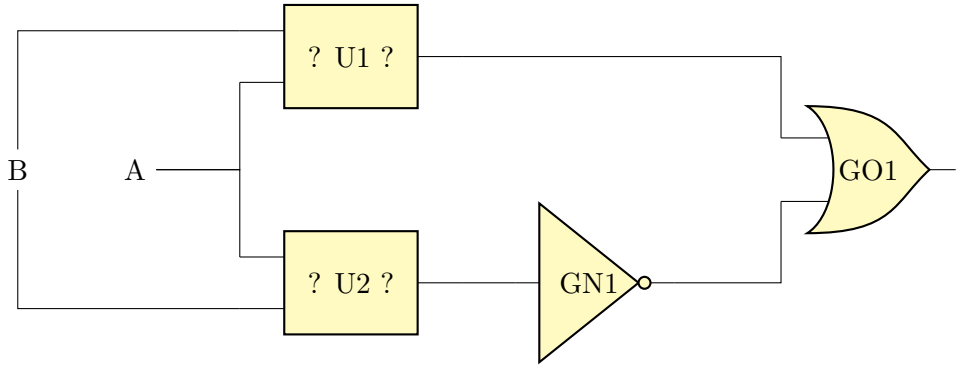


Figure 2: Partial circuit

A	B	U1	U2	GN1	GO1
0	0	0	0	?	?
0	1	?	1	?	0
1	0	?	?	0	0
1	1	1	?	0	?

Table 2: Partial Truth Table

[1] It is almost as if someone did this just so that Prof. Varma could make up a story for this problem.